## REMARKS

The Applicant thanks the Examiner for the careful examination of this application and respectfully requests the entry of the amendments indicated hereinabove.

Claims 1-29 are pending and rejected. Claims 1, 14, and 24 are amended and Claims 5 and 17 are cancelled hereinabove.

The Applicant respectfully traverses the drawing objection of paragraph 2 of page 2 of the Office Action. The Applicants submits that the label "$V_{DD}$ or $V_{DDI/O}$" of FIG. 2 is fully supported in paragraph 0037 of pages 19-20 of the Specification. Namely, paragraph 0037 states "Optionally, the first switch 210 and the second switch 220 may be connected to a voltage other than the high operating voltage $V_{DD}$. For example, the first switch 210 and the second switch 220 may be connected to the high input/output voltage $V_{DDI/O}$. Therefore, they are "interswitchable".

Regarding the drawing rejection in paragraph 3 of the Office Action on page 3 of "how the n-well may be connected to a high input/output voltage VDDI/O at about 1.8 volts while the high operating voltage VDD is at about 1.2 volts as

described in lines 21-23, page 19 of the specification", the Applicant has amended paragraph 0037 hereinabove to delete that sentence.

Furthermore, regarding the drawing rejection in paragraph 3 of the Office Action on page 3 "how the first switch 210 and the second switch 220 may be connected to the high input/output voltage $V_{DDI/O}$ as described in lines 1-3, page 20 of the present invention since all three transistors 210, 220 and 230 are commonly connected to $V_{DD}$ or $V_{DDI/O}$ without showing any circuit to break this connection", the Applicant notes that the "first and second switches, 210, 220, may be controlled by a first and second select signal SEL1, SEL2" (paragraph 0035) and the "third switch 230 may be controlled by a power-down signal...the power-down signal PD may go high and the third switch 230 is turned-off" (paragraph 0034) (see also FIG. 2 and paragraph 0036).

The Applicant respectfully traverses the drawing objection of paragraph 4 of page 4 of the Office Action. Specifically, Claims 1, 14 and 24 positively recite that "said array high supply voltage $V_{ADD}$ and said array low supply voltage $V_{ASS}$ are provided concurrently." The Applicants submits that the quoted claim limitation is supported in FIG. 3 and also throughout the Specification; such as "both an array high supply voltage $V_{ADD}$ ...and an array low supply voltage $V_{ASS}$ ...are provided to the SRAM array during a sleep mode" (paragraph 0040) and "After providing both the array high supply voltage $V_{ADD}$ and an array low supply

voltage $V_{ASS}$" (paragraph 0042) (see also paragraphs 0025-0026 and 0028-0030). Claim 11 positively recites "said sleep mode voltage controller further provides a well voltage such that an n-channel back bias voltage, a p-channel back bias voltage and a voltage across a SRAM cell are all about a same voltage." Claim 11 is supported in the Specification in original Claim 11, in FIG. 4, and in paragraph 0030 "Thus, the SRAM array may have about 0.4 volts back bias on both the n-channel and the p-channel in addition to about 0.4 volts across the SRAM cell as shown in FIG. 4." Similarly, Claim 23 positively recites "providing a well voltage such that an n-channel back bias voltage, a p-channel back bias voltage and a voltage across a SRAM cell are all about a same voltage." Claim 23 is supported in the Specification in original Claim 23, in FIG. 4, and in paragraph 0030 "Thus, the SRAM array may have about 0.4 volts back bias on both the n-channel and the p-channel in addition to about 0.4 volts across the SRAM cell as shown in FIG. 4." Claim 12 positively recites "said sleep mode voltage controller provides said array high supply voltage $V_{ADD}$ and said array low supply voltage $V_{ASS}$ based on a minimum voltage across said SRAM array that is sufficient for data retention." Claim 12 is supported in FIG. 3 and in paragraph 0043 "A test may be performed to determine a minimum voltage to maintain across the cell to retain data or to verify that the voltage across the cell is sufficient to retain data. The SRAM array voltages may be based on minimum cell voltage for data retention." (See also paragraphs 0006 and 0025.) Claim 13 positively recites "said sleep mode voltage controller

provides said array high supply voltage $V_{ADD}$ and said array low supply voltage $V_{ASS}$ based on a minimum voltage across said SRAM array that is sufficient for data retention and minimizing a total leakage current." Claim 13 is supported in FIG. 3 and in paragraph 0043 "After adjusting the array high supply voltage $V_{ADD}$ and the array low supply voltage $V_{ASS}$, the array high supply voltage $V_{ADD}$ and the array low supply voltage $V_{ASS}$ are refined based on a diode leakage current in a step 340. For example, if n-channel diode leakage current is high, the array low supply voltage $V_{ASS}$ may not be raised as much. Also, if the p-channel diode leakage current is high, the array high supply voltage $V_{ADD}$ may not be raised as much...A test may be performed to determine a minimum voltage to maintain across the cell to retain data or to verify that the voltage across the cell is sufficient to retain data. The SRAM array voltages may be based on minimum cell voltage for data retention." (See also paragraphs 0006 and 0025.)

The Applicant respectfully traverses the Specification objection in paragraph 5 of page 5 of the Office Action. Specifically, Claims 1, 14 and 24 positively recite that "said array high supply voltage $V_{ADD}$ and said array low supply voltage $V_{ASS}$ are provided concurrently." The Applicants submits that the quoted claim limitation is supported in FIG. 3 and also throughout the Specification; such as "both an array high supply voltage $V_{ADD}$ ...and an array low supply voltage $V_{ASS}$ ...are provided to the SRAM array during a sleep mode" (paragraph 0040) and "After providing both the array high supply voltage $V_{ADD}$

and an array low supply voltage $V_{ASS}$" (paragraph 0042) (see also paragraphs 0025-0026 and 0028-0030). Moreover, the Office Action asserts (pages 6-7) that if a drawing (such as the Applicant's FIG. 2) that shows voltages inputs on separate terminals that they are "inherently provided concurrently".

Amended independent Claim 1 positively recites that the sleep mode voltage controller provides the array high supply voltage $V_{ADD}$ and the array low supply voltage $V_{ASS}$ based on transistor parameters. These advantageously claimed features are not taught or suggested by the patent granted to Deng et al. (column 6 lines 16-42).

The Applicant respectfully traverses the statement in the Office Action (page 7) that "since the SRAM array 110 does have n-well, therefore, it also inherently must have a substrate at a voltage which also inherently must be equivalent to the low operating supply voltage Vss as well known in the art." The Applicant submits that it is well known in the art to have a substrate voltage different than $V_{SS}$ (to adjust for variations in the threshold voltage caused by process variations). (See also FIG. 2.)

Therefore, the Applicant respectfully traverses the Examiner's rejection of Claim 1 and respectfully asserts that Claim 1 is patentable over Deng et al. Furthermore, Claims 2-4 and 6-13 are allowable for depending on allowable

independent Claim 1 and, in combination, including limitations not taught or described in the reference of record.

Amended independent Claim 14 positively recites that providing the array high supply voltage $V_{ADD}$ and the array low supply voltage $V_{ASS}$ is based on transistor parameters. These advantageously claimed features are not taught or suggested by the patent granted to Deng et al. (column 6 lines 16-42).

Therefore, the Applicant respectfully traverses the Examiner's rejection of Claim 14 and respectfully asserts that Claim 14 is patentable over Deng et al. Furthermore, Claims 15-16 and 18-23 are allowable for depending on allowable independent Claim 14 and, in combination, including limitations not taught or described in the reference of record.

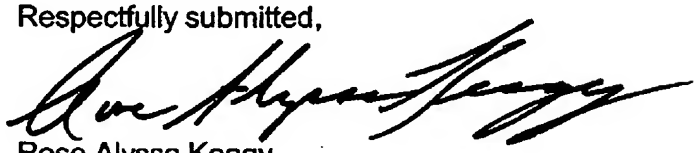
Amended independent Claim 24 positively recites that sleep mode voltage controller provides the array high supply voltage $V_{ADD}$ and the array low supply voltage $V_{ASS}$ are based on transistor parameters. These advantageously claimed features are not taught or suggested by the patent granted to Deng et al. (column 6 lines 16-42).

Therefore, the Applicant respectfully traverses the Examiner's rejection of Claim 24 and respectfully asserts that Claim 24 is patentable over Deng et al.

Furthermore, Claims 25-29 are allowable for depending on allowable independent Claim 24 and, in combination, including limitations not taught or described in the reference of record.

For the reasons stated above, this application is believed to be in condition for allowance. Reexamination and reconsideration is requested.

Respectfully submitted,



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